UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/776,250 | 02/12/2004 | Kazumasa Ando | 248806US2TTC | 4164 |

22850 7590 08/05/2005

OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

| EXAMINER | |
|---|---|
| NGUYEN, LONG T | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2816 | |

DATE MAILED: 08/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/776,250 | ANDO, KAZUMASA | |
| | Examiner | Art Unit | |
| | Long Nguyen | 2816 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *26 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 February 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/12/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Drawings*

1. The drawings are objected to because Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

The drawings are also objected to because the black-boxes in Figure 2 have not been provided with text label.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### *Claim Objections*

2. Claims 1-17 are objected to because of the following informalities:

Claim 1, line 7-8 of the claim, "or the current block" should be deleted.

Claim 1, line 8 of the claim, "a source or" should be deleted.

Claim 1, line 10 of the claim, "by" should be changed to --in response to--.

Claim 1, line 14 of the claim, "when" should be changed to --in response to--.

Claims 2-7 are objected to because they include the informalities of claim 1.

Claim 2, line 4, "the source or the drain" should be changed to --a source--.

Claim 3, lines 3 and 8, "capable of operating" should be changed to --operates-- since 'capable of' is not a positive recitation of the invention.

Claim 3, line 16, "a potential" should be changed to --the potential--.

Claim 5, line 1-3, "further comprising an output retainer including the output circuit and the retaining circuit," should be changed to --wherein the output circuit connected to the retaining circuit to form an output retainer circuit, and--.

Claim 6, line 2, it is suggest to change "both" to --each of the--.

Claim 6, line 3, "include CMOS inverters" is suggested to be changed to --includes a CMOS inverter--.

Claim 8, line 12 of the claim, "or the current block" should be deleted.

Claim 8, line 12 of the claim, "a source or" should be deleted.

Claim 8, line 15 of the claim, "by" should be changed to --in response to--.

Claim 8, line 19 of the claim, "when" should be changed to --in response to--.

Claims 9-17 are objected to because they include the informalities of claim 1.

Claim 11, line 4, "the source or the drain" should be changed to --a source--.

Claim 12, lines 3 and 8, "capable of operating" should be changed to --operates-- since 'capable of' is not a positive recitation of the invention.

Claim 12, line 16, "a potential" should be changed to --the potential--.

Claim 14, line 2-3, "wherein the level shifter further comprising an output retainer including the output circuit and the retaining circuit," should be changed to --wherein the output circuit connected to the retaining circuit to form an output retainer circuit, and--.

Claim 15, line 2, it is suggest to change "both" to --each of the--.

Claim 15, line 3, "include CMOS inverters" is suggested to be changed to --includes a CMOS inverter--.

Appropriate correction is required.

***Claim Rejections - 35 USC § 112***

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 3, 7, 12 and 16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 3, this claim is indefinite because it is not clear which one of the transistors recited in this claim is for the "first transistor" which having its gate receives the input signal (recited in independent claim 1).

With respect to claim 7, this claim is indefinite because it is not understood what applicant means by "time required for the returning by the output circuit and the feedback circuit" recited on line 2-3. Also, "the returning" lacks antecedent basis and it is not clear what it is referred too. Further, "the feedback circuit" lacks antecedent basis since "a feedback circuit" is recited in claim 5, so it appears that this claim should depend on claim 5 instead of claim 4.

With respect to claim 12, this claim is indefinite because it is not clear which one of the transistors recited in this claim is for the "first transistor" which having its gate receives the input signal (recited in independent claim 8).

Claim 16 is indefinite for the same reason as discussed in claim 7.

***Claim Rejections - 35 USC § 102***

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Maejima et al. (USP 6,791,392).

With respect to claims 1-7, Figure 3 of the Maejima et al. reference discloses a voltage level shifter circuit, which includes: a level changer (IV1, IV2, DT, TP1, TP2, TN1, TN2, TN31, TN32) having a current block (transistors TN31 and TN32) and a first transistor (either transistor TN1 or TN2); an input signal (IN); a low power voltage supply (VDDL); a high power voltage supply (VDDH); a reference potential (ground); an output circuit (CMOS inverter IV3); a retaining circuit (CMOS inverter IV4, which is a feedback circuit from the output of the output circuit to the output of the level changer, and the connection of the output circuit IV3 and the feedback circuit IV4 forms an output retainer circuit). Note that the level changer circuit (IV1, IV2, DT, TP1, TP2, TN1, TN2, TN31, TN32) includes: a first input circuit (IV1), a second input circuit (IV2), a first NMOS (TN1), a second NMOS (TN2), a first PMOS (TP1), a second PMOS

(TP2), and the current block (TN31-TN32) including a third NMOS (TN31) and a fourth NMOS (TN32). Also note for claim 7, because the structure of the level shifter in Figure 3 of the Maejima reference is substantially similar as applicant's invention so the limitation regarding the timing operation in this claim is also met.

With respect to claims 8-17, the Maejima et al. reference (Col. 1, lines 9-13) discloses a system, which includes: a peripheral circuit (the one circuit system, see Col. 1, lines 9-13), a voltage level shifter circuit (the level shift circuit which is shown in Figure 3), and an internal circuit (the another system, see Col. 1, lines 9-13), wherein the voltage level shifter circuit comprises: a level changer (IV1, IV2, DT, TP1, TP2, TN1, TN2, TN31, TN32) having a current block (transistors TN31 and TN32) and a first transistor (either transistor TN1 or TN2); an input signal (IN); a low power voltage supply (VDDL); a high power voltage supply (VDDH); a reference potential (ground); an output circuit (CMOS inverter IV3); a retaining circuit (CMOS inverter IV4, which is a feedback circuit from the output of the output circuit to the output of the level changer, and the connection of the output circuit IV3 and the feedback circuit IV4 forms an output retainer circuit). Note that the level changer circuit (IV1, IV2, DT, TP1, TP2, TN1, TN2, TN31, TN32) includes: a first input circuit (IV1), a second input circuit (IV2), a first NMOS (TN1), a second NMOS (TN2), a first PMOS (TP1), a second PMOS (TP2), and the current block (TN31-TN32) including a third NMOS (TN31) and a fourth NMOS (TN32). Also note, for claim 10, it is clear from the operation of the circuitry Maejima et al. reference that when the there is no power supply to the system (i.e., power supply is 0V) then the system is not operated, so the system is in standby period, and when there is power supply to the system then the system is in operation period; so the peripheral circuit (the one circuit system) is in standby when the

there is no power to the low supply voltage (i.e., VDDL is 0V which is the reference potential). Also note for claim 16, because the structure of the level shifter in Figure 3 of the Maejima reference is substantially similar as applicant's invention so the limitation regarding the timing operation in this claim is also met. Also note, in claim 17, for broadest reasonable interpretation, both the level shifter (Figure 3) and the another circuit system (Col. 1, lines 9-13) are reasonable to be considered to be a microcomputer (i.e., the microcomputer comprises the level shifter (Figure 3) and the another circuit system).

***Conclusion***

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Thursday from 8:00am to 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LONG NGUYEN
PRIMARY EXAMINER